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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Edward A. Schrock et al.
Title: METHOD FOR ATTACHING A SEMICONDUCTOR DIE TO A SUBSTRATE
Attorney Docket No.: 303.527US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X Return postcard.
X **DIVISIONAL** of prior Patent Application No. 09/227,942 (under 37 CFR § 1.53(b)) comprising:
  X Specification (30 pgs, including claims numbered 1 through 57 and a 1 page Abstract).
  X Formal Drawing(s) (4 sheets).
  X Copy of signed Declaration (3 pgs) from prior application.
  X Copy of Power of Attorney from prior application (1 pg.)
  X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
  X Check in the amount of $1,152.00 to pay the filing fee.
X Prior application is assigned of record to Micron Technology, Inc. .
X Information Disclosure Statement (1 pg), Form 1449 (2 pgs). References NOT enclosed, cited in prior application.
X Preliminary Amendment (2 pgs).

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	24 - 20 =	4	x 18 =	**$72.00**
INDEPENDENT CLAIMS	8 - 3 =	5	x 78 =	**$390.00**
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				**$0.00**
BASIC FEE				**$690.00**
TOTAL				**$1,152.00**

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EL517792744US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Edward A. Schrock et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.527US2
Title:	METHOD FOR ATTACHING A SEMICONDUCTOR DIE TO A SUBSTRATE	

PRELIMINARY AMENDMENT

BOX PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified patent application as follows:

IN THE SPECIFICATION

On page 1, after the title, please insert the following:

-- Cross-Reference to Related Applications

This application is a Division of U.S. Patent Application No. 09/227,942, filed January 11, 1999, the specification of which is hereby incorporated by reference.--

IN THE CLAIMS

Please cancel claims 1 - 33 without prejudice or disclaimer.

REMARKS

Claims 1 - 33 having been canceled, claims 34 - 57 are now pending.

The specification is amended to add a cross reference to the prior application.

The application filing fee as calculated on the application transmittal sheet reflects the amendments to the claims described above.

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application.

Respectfully submitted,

EDWARD A. SCHROCK ET AL.

By their Representatives,

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Method for Attaching a Semiconductor Die to a Substrate

Technical Field

This invention relates to semiconductor manufacturing and packaging. Particularly, it relates to a method for attaching a semiconductor die directly to an organic substrate such as a printed circuit board.

Background of the Invention

In the final stages of semiconductor manufacturing, a semiconductor "chip" or die is typically enclosed within a sealed package. The primary purpose of the semiconductor package is to provide a lead system for electrically and mechanically connecting the circuits on the die to a supporting structure such as a printed circuit board (PCB). Without the lead system, electrical connections to the die are made difficult by the fragile structure of the die face. The package also provides physical and environmental (e.g., moisture, chemical) protection and serves to dissipate heat from the die.

The conventional semiconductor packaging process starts by securing the die to a mounting paddle of a metal lead frame with a suitable adhesive. Electrical connections between bond pads on the face of the die and connections on the leads are then made using fine bond wires. A protective coating may be applied to portions of the die, bonding wires, and lead frame. The package is then encapsulated in a plastic or ceramic material from which the leads extend outwardly therefrom. The package may be trimmed and the leads formed to achieve the desired configuration.

A variation of conventional packaging is known as lead-on-chip (LOC) packaging. LOC differs in that the LOC lead frame has no mounting paddle. The leads of the lead frame attach directly to the face of the die and support the die

during the encapsulation process. LOC results in improved heat transfer and shorter bond wire length.

While both of these packaging methods have proven reliable, drawbacks exist. First, the encapsulation process adds cost to the finished semiconductor package. In addition, the equipment necessary for encapsulation is highly specialized and expensive. Finally, an encapsulated die is substantially larger and heavier than the die in its unpackaged state. As demand for smaller, more powerful electronic devices grows, semiconductor manufacturers are constantly seeking to increase semiconductor population within a given volume. Accordingly, the size of the semiconductor package becomes a significant concern.

To overcome these problems, alternatives to standard packaging have emerged. One such alternative is to eliminate the encapsulant and metal lead system altogether and attach the die directly to a PCB substrate. The resulting "chip-sized package" (CSP) may, in turn, may be attached through various means to other components including other printed circuit boards. By eliminating the die package and metal lead system, the die has a significantly smaller footprint (and volume). Thus, denser mounting may be achieved.

Bare die attachment to a PCB substrate generally involves first mounting the die to a die attach area on the substrate. The bond pads on the die face may then be wire bonded to connection points on the substrate using gold or aluminum wire. Or, as an alternative to wire bonding, the die may have a series of solder bumps on its face, which, when placed face down, contact connection points on the substrate. Heat or ultrasonic energy may be used to secure the solder bumps to the substrate. Since this process (often referred to as "flip chip bonding") requires specialized equipment, wire bonding remains the predominant and economically preferred method of die interconnection.

Typically, an encapsulant is applied to the bond wire area to protect the bond wires and their connections. However, this encapsulant is typically a liquid material

or "glob-top" applied locally and, thus, its application is not as complex or as costly as conventional encapsulation. Likewise, glob-top provides negligible volumetric increase to the die and substrate.

Since the CSP package has no metal lead system, an alternative method of external electrical and mechanical connection must be provided. The package may, for example, include a fine-pitch "ball grid array" or BGA. A BGA is an array of solder bumps or balls on a side of the PCB opposite the die attach area. Each ball is electrically connected through a conductive trace in the substrate to a wire bond connection point which, in turn, is wire bonded to the die. To mount the BGA package, the solder bumps contact conductive points on the receiving component and heat is applied to reflow the bumps. Other connection methods such as a "pin grid array" or PGA may be used. A PGA has a series of pins extending outwardly from the substrate rather than solder bumps. The pins are mechanically received in apertures on the receiving component. Accordingly, with CSP applications, the substrate itself must incorporate the lead system for electrical connection to the die.

While CSP reduces the bulky footprint common with conventional die packaging, attaching dice directly to PCBs introduces problems. One area of particular concern is the adhesive used to attach the die. The adhesive must physically secure the die and firmly retain it during all subsequent manufacturing operations (e.g., wire-bonding, glob-top curing, soldering). Generally speaking, die attach adhesives fall into one of two categories: tape and paste. In LOC packaging, adhesive tape or film is sometimes used to secure the die to the metal lead frame. This tape is typically a thermoplastic material such as polyimide film requiring high temperature processing. Often, lamination of LOC tape requires temperatures ranging from 325 - 400 deg C. While the lead frame and other components involved in conventional packaging are capable of this high thermal processing, organic substrates are not. Specifically, the substrate may severely outgas and degrade at temperatures well below 325 deg C. For this reason, paste or resin adhesives

having substantially lower processing temperatures have been developed for use with organic substrates. While satisfactory in addressing the thermal processing issue, paste adhesives have inherent drawbacks.

For example, due to the viscous properties of the paste, it tends to "bleed" outwardly from where it is applied. In some instances, the paste may migrate to the wire bond area (or other non-solder masked area). When this occurs, the package is typically rejected. Careful manufacturing control is thus necessary to prevent paste bleed.

Another problem associated with the viscous properties of paste adhesives is bond line thickness and bond area coverage. Without maintaining an even paste thickness, the die may seat in a non-parallel orientation relative to the substrate. When this occurs, damage to the edge of the die and/or the substrate may occur.

A related problem caused by reduced bond line thickness concerns the glob-top or over-mold material. Such materials may contain filler particles that can contact and damage the die face. Increased bond line thickness has been found to reduce this occurrence. However, as discussed above, bond line thickness is difficult to control with paste. Simply adding more paste generally results in increased paste displacement rather than greater bond line thickness.

Yet another problem related to the viscous characteristics of the paste is voiding. Due to the consistency of the paste and the inclusion therein of solvent diluents, voids may form during paste dispensing. These voids increase outgassing during subsequent thermal processing. Outgassing may adversely affect wire bond effectiveness and glob-top adhesion.

Still yet another drawback to paste adhesives is the limitations inherent in dispensing the paste. Specifically, paste is limited by filler size and distribution to accomplish certain flow characteristics necessary for dispensing. Because of the method in which paste is dispensed, the rheological properties of the paste must fall within certain defined limits. Particularly, the filler material, size, distribution, and

percentage within the paste is critical to provide effective flow of the adhesive. Accordingly, filler must be selected for its rheology characteristics rather than for its adhesive or mechanical properties.

Paste also requires curing. The introduction of heat into the lamination process may create thermal stresses into the bond line due to differing coefficients of thermal expansion (CTE) between the adhesive and the adherents. This may weaken the adhesive bond or warp the substrate.

Another problem with paste adhesive in die attach applications is that it is not in-line processable. Paste must be dispensed from above the substrate. Currently available die attachment machines, however, attach the die from beneath the substrate. Therefore, the substrate must be inverted after the paste is dispensed and before the die is attached. This adds another step in the manufacturing process which further increases production time and cost.

Thus, there are unresolved issues, some of which are enumerated above, with present die attachment technology. Specifically, an improved method for attaching dice directly to organic substrates is needed.

Summary of the Invention

An improved method of attaching a semiconductor die to an organic substrate and an improved semiconductor package are provided herein. The package comprises a semiconductor die, an organic support structure, and an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape has an adhesive such as pressure sensitive adhesives, thermoplastic adhesives, thermoset adhesives or the like. The organic support structure may be a printed circuit board. A method of attaching a semiconductor die to an organic support structure comprises selecting a two-sided adhesive tape having an adhesive such as a pressure sensitive adhesive, thermoplastic adhesive, thermoset adhesive, or the like; affixing a first side of the two-sided adhesive tape to a surface

of the organic support structure; and affixing a face of the semiconductor die to a second side of the adhesive tape.

The adhesive tape may be a single adhesive layer or a multi-layer film. In one embodiment, the adhesive tape comprises a first adhesive layer adjacent to the organic support structure, a second adhesive layer adjacent to the semiconductor die, and a carrier layer intermediate the first and second adhesive layers. The first adhesive layer may have a first coefficient of thermal expansion substantially identical to that of the support structure. Similarly, the second adhesive layer may have a second coefficient of thermal expansion substantially identical to that of the semiconductor die. The intermediate carrier layer may be a polyimide film. The organic support structure may additionally comprise a feature that permits interconnecting the package to other electronic components. In one embodiment, the interconnecting feature is a BGA.

Another method for attaching a die to an organic support structure is disclosed generally comprising affixing a first side of a two-sided adhesive tape to the surface of the organic support structure; elevating the temperature of the tape to activate the adhesive; applying pressure to the tape and organic support structure to laminate the first side of the adhesive tape to the organic support structure; affixing a face of the semiconductor die to the second side of the adhesive tape; elevating the temperature of the tape to activate the adhesive; and applying pressure to the die and organic support structure to laminate the second side of the adhesive tape to the die.

Furthermore, the bond pads may be electrically connected to the lead connections on the organic support structure. An encapsulating material may then be formed around portions of the die and organic support structure. In one embodiment, the encapsulating material is a curable glob-top occupying negligible volume.

The support structure may be trimmed to form a BGA package comprising the die and the organic support structure, with the encapsulating material protecting the bond pads, bond wires and lead connections.

The BGA package may be interconnected to a receiving electronic component such as a system PCB. The finished BGA package is smaller and more economical to produce than conventional encapsulated packages. Additionally, the adhesive tape described herein is advantageous over the paste adhesives currently used to attach dice to organic substrates.

Brief Description of the Drawings

The invention described herein will be further characterized with reference to the drawings, wherein:

Figure 1 is an enlarged side view of a semiconductor package of the present invention;

Figure 2 is an exploded perspective view of a one embodiment of the PCB substrate showing a plurality of die receiving areas;

Figure 3 is a plan view of a semiconductor die attached to a PCB substrate according to one embodiment of the present invention;

Figure 4 is an enlarged side view of one embodiment of the adhesive tape of the present invention;

Figure 5a-5f are schematic side elevation views illustrating the steps for packaging a semiconductor die according to one embodiment of the present invention; and

Figure 6 is a diagrammatic view of a system having a memory device incorporating a semiconductor package according to one embodiment of the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Generally, the present invention is directed to an improved semiconductor package and an improved method for attaching a semiconductor package to a support structure. Particularly, the invention is directed to support structures that are incompatible with conventional thermal processing operations, i.e., substrates that may degrade at lower temperatures than conventional substrate materials. This category of support structures will be hereinafter referred to generally as organic support structures/substrates and specifically as printed circuit board (PCB) substrates. Those skilled in the art, however, will realize that other substrate materials are also within the scope of the invention. Thus, references to organic support structures and PCBs are not intended to limit the scope of the invention.

Referring generally to Figure 1, a die 10 and a PCB substrate 12 are shown. The die 10 is generally a flat, rectangular device having a plurality of integrated circuits (not shown) formed on a side of the die. In one embodiment, the circuits are disposed on a face side 14. A plurality of center bond pads 16 are located on the face 14 and form the electrical connections to the die's integrated circuits. While shown with circuits and bond pads on the face 14, those skilled in the art will realize that the circuits and bond pads may be disposed on a back side 15 of the die. In the latter case, apertures (not shown) through the die permit electrical connection to the die's integrated circuits.

Referring now to Figure 2, the PCB 12 may be a flexible board or film having side rails 18, 20 to support the substrate during manufacture. In one

embodiment, the substrate comprises a BT (bismaleimide triazine) resin core. In order to increase manufacturing efficiency, the substrate 12 may be a continuous sheet or film capable of accommodating a plurality of dice. A series of indexing openings 22 may be used to aid automation machinery. The PCB 12 additionally has a first side 24 having a die attach area 26 and a second side 28 (best shown in Figure 3) having a plurality of lead connection pads 30. Still referring to Figure 2, the die attach area 26 is rectangular and substantially identical in size to the die 10. The die attach area may be slightly recessed in the substrate or it may be formed on the substrate surface. A rectangular aperture 32 is formed through the center of the die attach area 26. A slot 33 separates each die attach area from the next. The purpose of the aperture 32 and slot 33 will become apparent shortly.

Referring to Figure 3, the second side 28 of the PCB 12 comprises a ball grid array (BGA) 34. The BGA permits electrical and mechanical interconnection of the die 10 and substrate 12 to other electronic components including other circuit boards. The BGA 34 comprises an array of solder bumps or balls 36 (which may be formed during a subsequent manufacturing operation) connected by traces to the connection pads 30. While a BGA is represented in this embodiment, other connection methods (e.g., mechanical) are also considered to be within the scope of the invention. The connection pads 30, in turn, are connected by a series of fine bond wires 38 to the bond pads 16 (best shown in Figure 1). Thus, the BGA 34 provides a lead system for electrical connection to the integrated circuits on the die face 14.

Unlike a metal lead frame, the PCB 12 is an organic material. As such, it is incapable of withstanding the high thermal processing temperatures often associated with conventional (i.e., lead fame) packaging. Accordingly, thermal processing temperatures must remain relatively low.

As best viewed in Figure 1, an adhesive tape 40 lies intermediate to the die 10 and PCB 12. The adhesive tape 40, which is shown in detail in Figure 4, is a

two-sided dielectric material having a first side 42 that adheres to the die attach area 26 and a second side 44 that adheres to the die 10. In one embodiment, the adhesive tape 40 comprises two strips, one on each side of the aperture 32. The tape 40 may be a single polymeric adhesive layer or, alternatively, it may be a multi-layer material as shown in Figure 4. With the latter, the tape comprises a first adhesive layer 46 proximate the substrate 12, a second adhesive layer 48 proximate the die 10, and an intermediate layer 50. Other single and multi-layered tapes are also considered to fall within the scope of the invention.

The adhesive layer(s) 46, 48 may be responsive to heat, pressure, or both. In one embodiment, the heat responsive component is a thermoset material. The thermoset material may be a "B-stageable" material (i.e., having an intermediate stage in which the material remains wholly or partially plastic and fusible so that it softens when heated). In yet another embodiment, the heat responsive component is a thermoplastic material.

Referring generally to Figure 4, an embodiment utilizing a tri-layer tape will now be described. While dimensional information is provided, it is to be understood that tapes of other layer configurations, sizes, thicknesses, and materials are also contemplated to be within the scope of the invention.

Layers 46, 48 are comprised of a CTBN (Carboxyl Terminated Acrylonitrile-Butadiene) modified epoxy resin formed into layers approximately .0005 inches thick. The resulting adhesive is a thermoset material that laminates at approximately 100 deg C. Complete crosslinking of the material occurs during a higher post-cure temperature as further described herein. The intermediate layer is preferably a polyimide carrier film such as UPILEX® (commercially available from UBE Industries Ltd) or KAPTON® (available from Dupont). In one embodiment, the carrier layer 50 is approximately .002 inches thick. The tri-layer tape as described herein was developed per Applicant's specifications and is presently produced by Ablestik Electronic Materials & Adhesives under part number RP444-3.

Having described the substrate 12, die 10, and adhesive tape 40, a method for attaching the die to the substrate will now be described. The order of the steps may be rearranged to some degree to better accommodate manufacturing processes. Similarly, the processing temperatures, times, and cures discussed herein may be modified to better suite a particular application. Finally, while the curing methods described are temperature processes, other curing methods (e.g., radiation) are also within the scope of the invention.

The method makes reference to various manufacturing "stations" that accomplish specific tasks. These stations are common and well known in the art and are thus perceived to require no detailed explanation. However, the particular step accomplished by each station is described in sufficient detail to enable one of skill in the art to practice the invention.

With reference to Figure 5, the substrate 12 is placed on an automated conveyor system with the first side 24 facing downwardly. The automated machinery then indexes the substrate 12 to a tape punch station. As shown in Figure 5a, the tape 40 is punched into two strips and the first side 42 is pressed against the die attach area 26 of the substrate 12. The tape 40 is heated momentarily to complete the lamination process. The heat applied is generally below that required to crosslink or set the adhesive. In one embodiment, pressure and 100 deg C heat are applied for 100 ms.

Referring now to Figure 5b, the substrate 12 is indexed to the die attach station where the die 10 is brought from beneath the substrate and the die face 14 is placed against the second side 44 of the tape. The die 10 is then pressed against the die attach area 26 with the tape 40 sandwiched therebetween. Once again, the adhesive is activated by heat and pressure. In one embodiment, pressure and 100 deg C heat is applied for 100 ms to laminate the tape 40 to the die 10. At this point, the die is physically attached to the PCB substrate 12. Unlike paste attachment, the

tape 40 will not bleed during lamination. Additionally, because the tape thickness is easily controlled during manufacture, bond line thickness is more easily controlled. Finally, the adhesive tape 40 permits the attachment of the die 10 without having to invert the substrate 12 as required with paste applications.

Referring now to Figures 5c, the substrate 12 and die 10 are then indexed to a wire bonding station wherein the bond pads 16 on the die face 14 are connected to the connection pads 30 on the substrate 12 with bond wires 38 passing through the aperture 32. Wire bonding can be accomplished with a wire bonder and conventional wire bonding methods. While wire bonding is the preferred method for electrically connecting the die to the substrate, other connection methods (e.g., mechanical, soldered) may also be employed.

Next, as shown in Figure 5d, an encapsulating material 52 is applied to the second side 28 of the PCB 12 in the wire bond area. The encapsulating material 52 covers the aperture 32, bond wires 38, connection pads 30 and a portion of the die face 14. The encapsulant 52 is preferably a glob-top material that adequately protects the bond pads and wire bonds without interfering with other components. The glob-top 52 does not appreciably increase the volume of the complete semiconductor package. It may be an epoxy, silicone or other commercially available material suitable for such purposes. The glob-top 52 may be applied by conventional methods such as dispensing the material from a needle apparatus directly over the wire bond area. In one embodiment, the glob-top is cured for 30 minutes at 150 deg C.

The substrate 12 is then flipped and a glob top 54 is applied to the perimeter of the back side (i.e., the side opposite face 14) of die 10 as shown in Figure 5e. The substrate 12 and die 10 then enter a post cure process. In one embodiment, the post cure is a two-step cure consisting of one hour at 110 deg C followed by one hour at

165 deg C. The post cure operation ensures proper evaporation of all solvents within the glob-top materials 52, 54. Additionally, the cure sets the adhesive layers 46, 48.

At the completion of the final cure, the substrate 12 with its attached die 10 may be sheared to form individually CSPs or plastic BGA (PBGA) packages 56 (see generally Figure 5f). The substrate 12 may be sheared along a line 58 between slots 33 as shown in Figure 2. The singular package 56 is then ready for attachment to other components.

Referring to Figure 5f, the package 56 of the present invention is shown just prior to attachment with a receiving component 60 such as another PCB. To attach the BGA package 56, the BGA solder balls 36 are added on the second side 28 of the substrate 12 and disposed at a height greater than that of the glob-top 52. Thus, the BGA solder balls 36 may contact the receiving substrate 60 without interference from the glob-top 52. To mount the singular BGA package 56 to the receiving component 60, it must first be accurately positioned relative to the component. The package 56 is then pressed against the receiving component 60 until the solder balls 36 contact the mating contacts on the component 60. The assembly may be heated until the solder balls begin to liquefy, thus securing the BGA package 56 to the component 60.

The receiving component 60 in one embodiment is a memory component as shown in Figure 6. The memory component 60 may comprise one or more of the BGA packages 56. The memory component 60 may be incorporated into an electronic device 62 which may incorporate a processor 64.

In an alternative embodiment, the thermosetting adhesive is a B-stageable material. A B-stageable material is actually a thermosetting material that is "re-meltable." That is, it has a first solid phase followed by a rubbery stage at elevated temperature, followed by yet another solid phase at an even higher temperature. The transition from the rubbery stage to the second solid phase is thermosetting.

However, prior to that, the material behaves similarly to a thermoplastic material. Thus, such a material would permit low lamination temperatures while providing high thermal stability.

While the adhesive tape of the present invention has been described as a heat and pressure activated thermoset material, other materials are also contemplated. For example, in another embodiment, each adhesive layer is formed of a pressure sensitive material. Pressure activated adhesives are particularly advantageous in eliminating bond line stress due to coefficient of thermal expansion (CTE) mismatch between the adhesive and the adherents. With temperature activated adhesives, CTE mismatch causes stress at the bond line during lamination because of the different expansion rates of the materials. By using a pressure activated adhesive, no heat is required for lamination. Thus, CTE mismatch is not an issue. By carefully selecting the pressure activated adhesive used, thermal bond line stress can also be minimized during subsequent temperature processing (e.g., wire bonding).

In yet another embodiment, the adhesive tape 40 is a hybrid between a thermoplastic and thermoset material. Unlike the thermoset material, the thermoplastic material is capable of being softened by increases in temperature and hardened by decreases in temperature. Thermoplastic tapes are currently available for LOC applications. This tape is typically a polyimide material requiring temperature processing in excess of 325 deg C. Accordingly, such tapes are ill-suited for use with organic substrates. However, a hybrid thermoplastic tape having a thermoset component therein is considered to fall within the scope of the present invention. The thermoset component of the tape is a material having a low thermal processing requirement. That is, the glass transition temperature (Tg) of the thermoset component is low, allowing the tape to laminate at low or ambient temperature. In one embodiment, the thermoset component has a Tg of approximately 30 deg C. The thermoplastic component of the tape, on the other hand, comprises a high Tg material providing high thermal stability for the

subsequent wire bonding and solder reflow operations. Accordingly, the hybrid tape would compromise the high Tg and low Tg characteristics in order to satisfy the competing requirements of the BGA substrate (i.e., low lamination temperature and high thermal stability). Currently available tapes do not address such competing requirements.

Thus, an improved method of mounting a semiconductor die to an organic substrate and an improved CSP are described herein. The tape used to mount the die to the substrate addresses many of the problems encountered with conventional paste attachment methods including but not limited to, elimination of resin bleed, improved bond line control, less die face damage due to glob-top filler particles, broader selection of available fillers, and improved in-line processing.

Preferred embodiments of the present invention are described above. Those skilled in the art will recognize that many embodiments are possible within the scope of the invention. Variations and modifications of the various parts and assemblies can certainly be made and still fall within the scope of the invention. Thus, the invention is limited only by the following claims, and equivalents thereto.

We claim:

1.) An integrated circuit package, comprising:

a semiconductor die;

an organic support structure; and

an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape comprises at least one adhesive selected from the group consisting essentially of pressure sensitive adhesives, thermoplastic adhesives, and thermoset adhesives.

2.) The integrated circuit package of claim 1, wherein the adhesive tape is a single adhesive layer.

3.) The integrated circuit package of claim 1, wherein the adhesive tape is a multi-layer tape.

4.) The integrated circuit package of claim 3, wherein the adhesive tape comprises:

a first adhesive layer adjacent to the organic support structure;

a second adhesive layer adjacent to the semiconductor die; and

a carrier layer intermediate the first and second adhesive layers.

5.) The integrated circuit package of claim 4, wherein the first adhesive layer has a first coefficient of thermal expansion substantially identical to that of the organic support structure.

6.) The integrated circuit package of claim 5, wherein the second adhesive layer has a second coefficient of thermal expansion substantially identical to that of the semiconductor die.

7.) An integrated circuit package, comprising:

a semiconductor die;

an organic support structure; and

an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape is comprised of a pressure sensitive adhesive.

8.) An integrated circuit package, comprising:

a semiconductor die;

an organic support structure; and

an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape is comprised of a thermoplastic adhesive.

9.) An integrated circuit package, comprising:

a semiconductor die;

an organic support structure; and

an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape is comprised of a pressure activated, thermoset adhesive.

10.) An integrated circuit package, comprising:

a semiconductor die;

an organic support structure; and

an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape is comprised of a thermoset adhesive.

11.) An integrated circuit package, comprising:

a semiconductor die;

an organic support structure having a die attach area for receiving the die; and

an adhesive tape disposed between the die attach area and the semiconductor die, wherein the adhesive tape comprises:

a first adhesive layer adjacent to the organic support structure;

a second adhesive layer adjacent to the semiconductor die; and

a carrier layer intermediate the first and second adhesive layers.

12.) The integrated circuit package of claim 11, wherein the first and second adhesive layers are comprised of a pressure activated material.

13.) The integrated circuit package of claim 11, wherein the first adhesive layer has a first coefficient of thermal expansion substantially identical to that of the organic support structure.

14.) The integrated circuit package of claim 11, wherein the second adhesive layer has a second coefficient of thermal expansion substantially identical to that of the semiconductor die.

15.) The integrated circuit package of claim 11, wherein the first and second adhesive layers are comprised of a thermoset material.

16.) The integrated circuit package of claim 11, wherein the first and second adhesive layers are comprised of a thermoplastic material.

17.) The integrated circuit package of claim 11, wherein the first and second adhesive layers are comprised of a pressure activated, thermoset material.

18.) The integrated circuit package of claim 11, wherein the carrier layer is comprised of a polyimide film.

19.) The integrated circuit package of claim 11, wherein the organic support structure is a PCB substrate.

20.) An integrated circuit package, comprising:

a semiconductor die having a face side and a back side wherein the face side comprises a plurality of bond pads;

an organic substrate having a first side and a second side, the first side having a die attach area for receiving the die and wherein the die attach area includes an aperture; and

an adhesive tape disposed between the die attach area and the semiconductor die, wherein the adhesive tape comprises:

a first adhesive layer adjacent to the organic support structure;

a second adhesive layer adjacent to the semiconductor die; and

a polyimide carrier layer intermediate the first and second adhesive layers.

21.) The integrated circuit package of claim 20 wherein the first and second adhesive layers comprise a pressure activated, thermoset material.

22.) The integrated circuit package of claim 21 wherein the die attach area is recessed relative the first side.

23.) The integrated circuit package of claim 22 wherein the adhesive tape is disposed in two strips on either side of the aperture.

24.) The integrated circuit package of claim 23 wherein the second side of the organic substrate additionally comprises:

a plurality of lead connections located proximate the aperture; and

means for interconnecting the circuit package.

25.) The integrated circuit package of claim 24 wherein the interconnecting means is a BGA located on the second side of the organic substrate.

26.) An integrated circuit package, comprising:

a semiconductor die having a face side and a back side wherein the face side comprises a plurality of bond pads;

an organic substrate having a first side and a second side, the first side having a recessed die attach area for receiving the die and wherein the die attach area includes an aperture, the second side having: a plurality of lead connections located proximate the aperture; and a BGA for interconnecting the circuit package; and

an adhesive tape disposed between the die attach area and the semiconductor die, the tape forming two strips, one on either side of the aperture, wherein the adhesive tape comprises:

a first adhesive layer adjacent to the organic support structure;

a second adhesive layer adjacent to the semiconductor die, wherein the first and second adhesive layers comprise a pressure activated, thermoset material; and

a polyimide carrier layer intermediate the first and second adhesive layers.

27.) The integrated circuit package of claim 26 wherein the bond pads on the die face side are connected to the lead connections by a series of bond wires passing through the aperture.

28.) The integrated circuit package of claim 27 further comprising an encapsulating material over the bond pads, bond wires, lead connections, and a portion of the substrate.

29.) The integrated circuit package of claim 28 wherein the encapsulating material comprises a curable glob-top.

30.) The integrated circuit package of claim 29 wherein the organic substrate is a PCB substrate.

31.) An integrated circuit package, comprising:

a semiconductor die having a face side and a back side wherein the face comprises a plurality of bond pads;

a PCB substrate having a first side and a second side, the first side having a die attach area for receiving the die and the second side having:

a plurality of lead connections electrically connected to the bond pads; and

a BGA providing external electrical connection to the package;

an adhesive tape disposed between the die attach area and the semiconductor die, wherein the adhesive tape comprises:

a first adhesive layer adjacent to the PCB substrate;

a second adhesive layer adjacent to the semiconductor die; and

a polyimide carrier layer intermediate the first and second adhesive layers; and

a receiving component providing the external electrical connection to the BGA.

32.) The circuit package of claim 31, wherein the first and second adhesive layers comprise a pressure activated, thermoset material.

33.) A system comprising:

a processor; and

a memory component operatively coupled to the processor comprising:

a semiconductor die;

an organic support structure; and

an adhesive tape disposed between the organic support structure and the semiconductor die, wherein the adhesive tape comprises at least one adhesive selected from the group consisting essentially of pressure sensitive adhesives, thermoplastic adhesives, and thermoset adhesives.

34.) A method of attaching a semiconductor die to an organic support structure, comprising:

selecting a two-sided adhesive tape having at least one adhesive selected from the group consisting essentially of pressure sensitive adhesives, thermoplastic adhesives, and thermoset adhesives;

affixing a first side of the two-sided adhesive tape to a surface of the organic support structure; and

affixing a face of the semiconductor die to a second side of the adhesive tape.

35.) A method of attaching a semiconductor die to an organic support structure, comprising:

affixing a first side of a two-sided adhesive tape to a surface of the organic support structure, wherein the adhesive tape comprises a pressure sensitive adhesive; and

affixing a face of the semiconductor die to a second side of the adhesive tape.

36.) A method of attaching a semiconductor die to an organic support structure, comprising:

affixing a first side of a two-sided adhesive tape to a surface of the organic support structure, wherein the adhesive tape comprises a thermoset adhesive; and

affixing a face of the semiconductor die to a second side of the adhesive tape.

37.) A method of attaching a semiconductor die to an organic support structure, comprising:

affixing a first side of a two-sided adhesive tape to a surface of the organic support structure, wherein the adhesive tape comprises a thermoplastic adhesive; and

affixing a face of the semiconductor die to a second side of the adhesive tape.

38.) A method of attaching a semiconductor die to an organic support structure, comprising:

affixing a first side of a two-sided adhesive tape to a surface of the organic support structure, wherein the adhesive tape comprises a pressure sensitive, thermoset adhesive; and

affixing a face of the semiconductor die to a second side of the adhesive tape.

39.) A method of attaching a semiconductor die to an organic support structure, comprising:

affixing a first side of a two-sided adhesive tape to a surface of the organic support structure, wherein the adhesive tape comprises a pressure sensitive, thermoset adhesive;

elevating the temperature to activate the first side of the adhesive tape;

applying pressure to the tape and organic support structure to laminate the adhesive tape to the organic support structure;

affixing a face of the semiconductor die to a second side of the adhesive tape;

elevating the temperature of the tape to activate the second side of the adhesive tape; and

applying pressure to the die and organic support structure to laminate the adhesive tape to the die.

40.) The method of claim 39 further comprising electrically connecting a plurality of bond pads on the die face with a plurality of lead connections on the organic support structure.

41.) The method of claim 40 wherein electrically connecting the bond pads to the lead connections comprises wire bonding bond wires to the bond pads and the lead connections.

42.) The method of claim 41 further comprising forming an encapsulating material around portions of the die and organic support structure.

43.) The method of claim 42 wherein the encapsulating material encapsulates the bond pads, bond wires, lead connections, and a portion of the die face and support structure.

44.) A method of attaching a semiconductor die to an organic support structure, comprising:

affixing a first side of a two-sided adhesive tape to a surface of the organic support structure, wherein the adhesive tape comprises a pressure sensitive, thermoset adhesive;

elevating the temperature of the tape to activate the first side of the adhesive tape;

applying pressure to the tape and organic support structure to laminate the adhesive tape to the organic support structure;

affixing a face of the semiconductor die to a second side of the adhesive tape;

elevating the temperature of the tape to activate the second side of the adhesive tape;

applying pressure to the die and organic support structure to laminate the adhesive tape to the die;

wire bonding bond wires to a plurality of bond pads on the die face with a plurality of lead connections on the organic support structure;

applying an encapsulating material over the bond pads, bond wires, lead connections, and a portion of the die face and support structure.

45.) The method of claim 44 wherein the encapsulating material comprises a curable glob-top formed by dispensing a viscous curable material.

46.) The method of claim 45 further comprising curing the encapsulating material.

47.) The method of claim 46 further comprising inverting the organic support structure and applying a second curable glob-top to a perimeter of a back side of the semiconductor die.

48.) The method of claim 47 further comprising curing the die and the organic support structure.

49.) The method of claim 48 further comprising trimming the organic support structure to form a BGA package.

50.) The method of claim 49 further comprising electrically interconnecting the BGA package to a receiving component.

51.) A method for fabricating a semiconductor package comprising:

providing a semiconductor die having a face and a plurality of bond pads;

providing an organic support structure comprising a die attach area and a plurality of lead connections;

providing a two-sided adhesive tape intermediate the die and the organic support structure to bond the die thereto; and

attaching a first side of the adhesive tape to the die attach area of the organic support structure and a second side of the adhesive tape to the die face.

52.) The method of claim 51 further comprising applying heat to laminate the tape to the die and the organic support structure.

53.) The method of claim 52 further comprising applying pressure to laminate the tape to the die and the organic support structure.

54.) The method of claim 53 further comprising electrically connecting the bond pads to the lead connections.

55.) The method of claim 54 wherein the electrical connection comprises connecting a series of bond wires to the bond pads and to the lead connections.

56.) The method of claim 55 further comprising applying a viscous material to cover the bond pads, lead connections, bond wires, and a portion of the organic support structure.

57.) The method of claim 56 wherein the viscous material is a curable glob-top.

Abstract

An improved method of attaching a semiconductor die to an organic substrate and an improved semiconductor package are herein disclosed. The die package comprises a die secured to a printed circuit board (PCB) with an adhesive tape. The adhesive tape may be of single or multi-layer construction. In one embodiment, a tri-layer tape is disclosed having a carrier layer sandwiched between two identical adhesive layers. In one embodiment, a method is disclosed utilizing a pressure sensitive, thermoset adhesive tape. In another embodiment, a method is disclosed utilizing a B-stageable thermoset adhesive. In yet another embodiment, a method using a pressure sensitive adhesive is disclosed. In still yet another embodiment, a method is disclosed wherein the adhesive is a hybrid material having both thermoset and thermoplastic components.

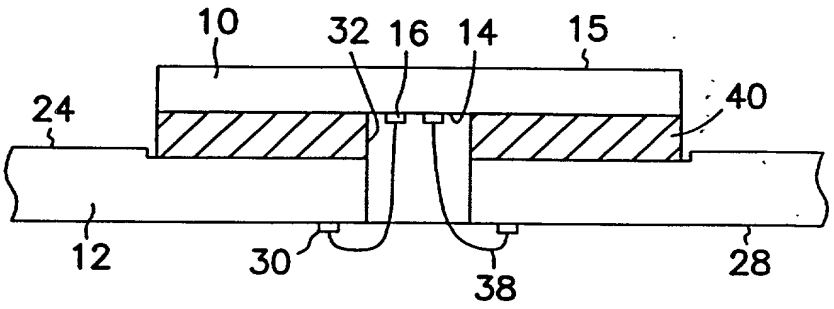
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FIG. 1

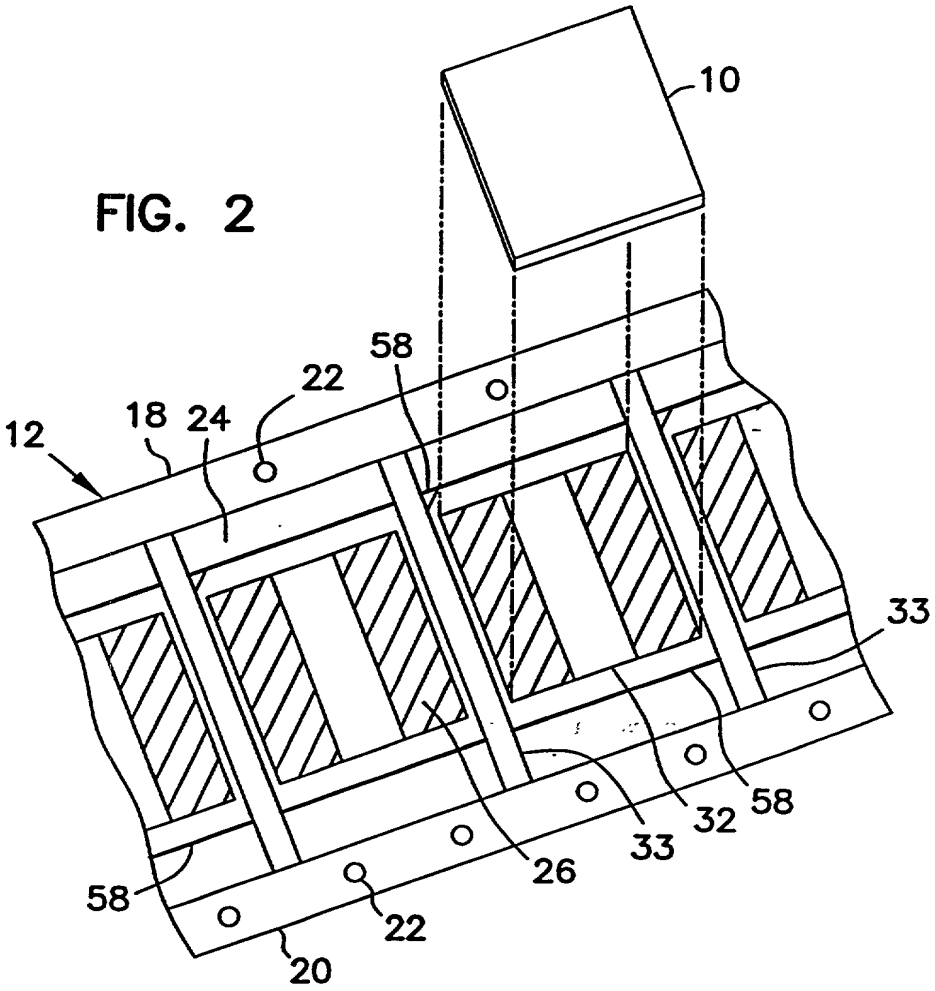
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FIG. 2

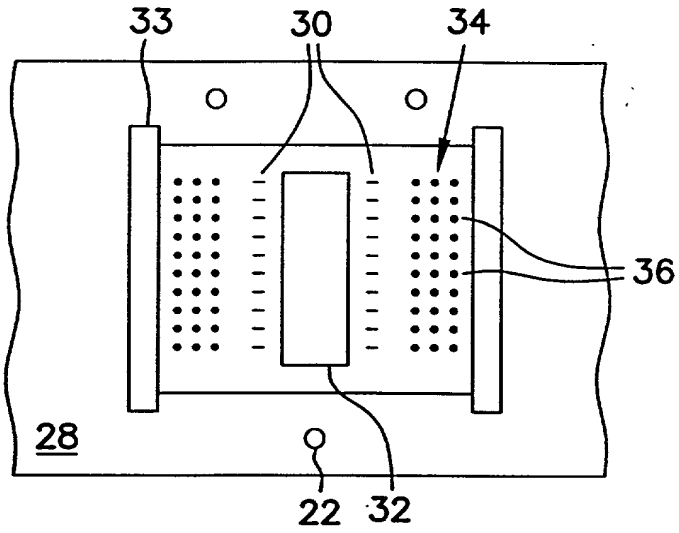


FIG. 3

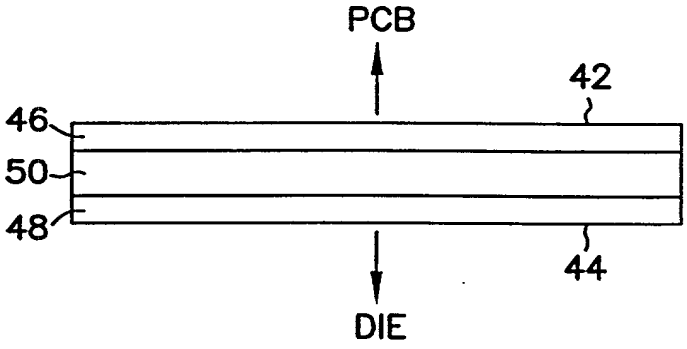


FIG. 4

FIG. 5a

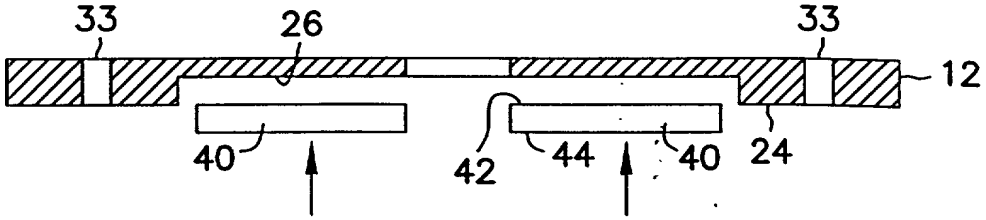


FIG. 5b

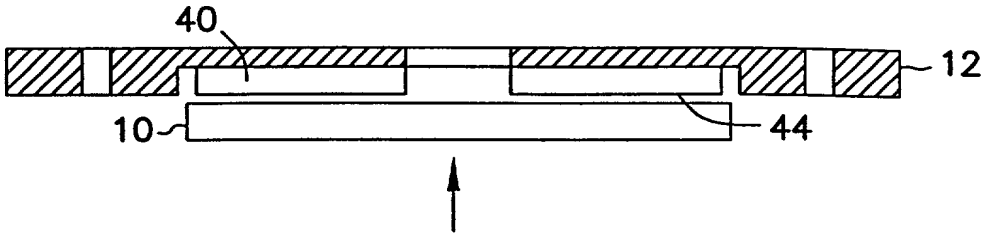


FIG. 5c

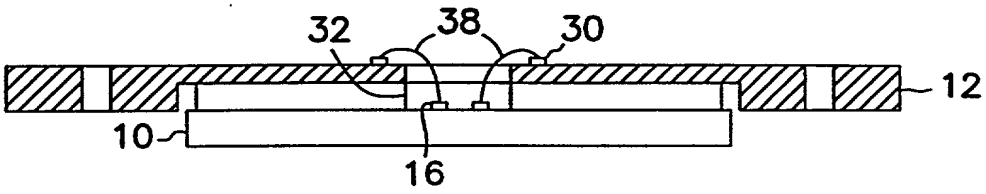


FIG. 5d

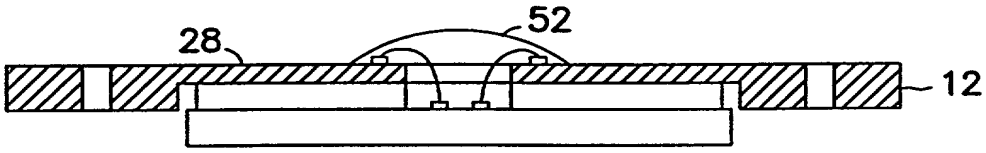


FIG. 5e

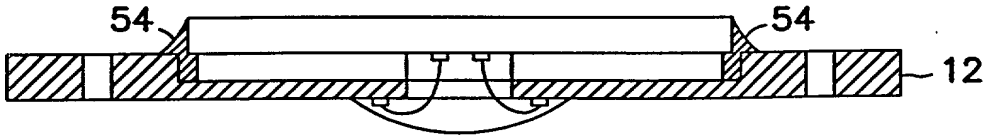
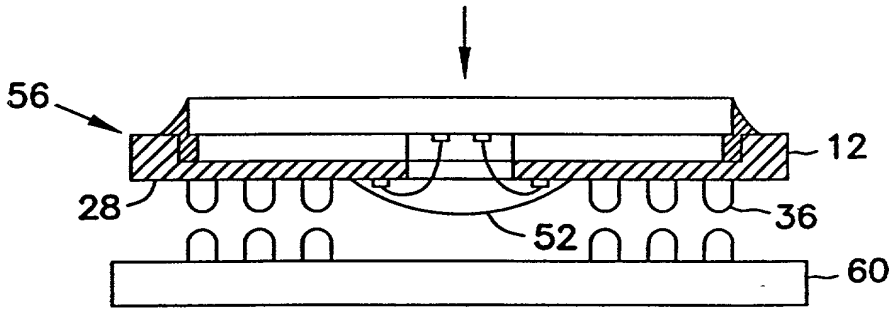


FIG. 5f



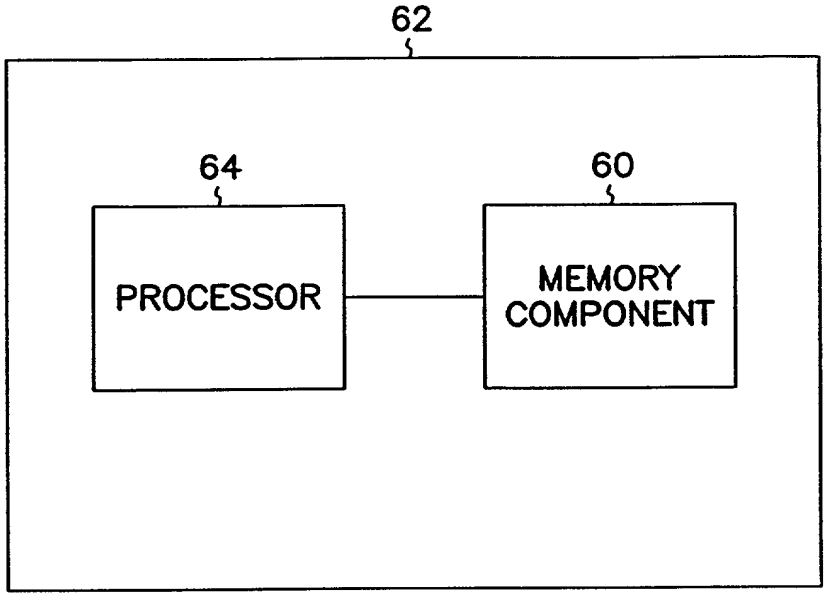


FIG. 6

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR ATTACHING A SEMICONDUCTOR DIE TO A SUBSTRATE .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: Edward A. Schrock Date: 12-30-98
Edward A. Schrock

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Signature: Tongbi Jiang Date: 12/30/98
Tongbi Jiang

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Edward A. Schrock et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.527US1	
Title:	METHOD FOR ATTACHING A SEMICONDUCTOR DIE TO A SUBSTRATE		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Matthew W.	Reg. No. P-43,459	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Anglin, J. Michael	Reg. No. 24,916	Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271
Arora, Suneel	Reg. No. 42,267	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. 42,858
Bianchi, Timothy E.	Reg. No. 39,610	Holloway, Sheryl S.	Reg. No. 37,850	Padys, Danny J.	Reg. No. 35,635
Billion, Richard E.	Reg. No. 32,836	Huebsch, Joseph C.	Reg. No. 42,673	Polglaze, Daniel J.	Reg. No. 39,801
Black, David W.	Reg. No. 42,331	Kalis, Janal M.	Reg. No. 37,650	Schwegman, Micheal L.	Reg. No. 25,816
Brennan, Thomas F.	Reg. No. 35,075	Klima-Silberg, Catherine I.	Reg. No. 40,052	Sieffert, Kent J.	Reg. No. 41,312
Brooks, Edward J., III	Reg. No. 40,925	Kluth, Daniel J.	Reg. No. 32,146	Slifer, Russell D.	Reg. No. 39,838
Clark, Barbara J.	Reg. No. 38,107	Lacy, Rodney L.	Reg. No. 41,136	Terry, Kathleen R.	Reg. No. 31,884
Drake, Eduardo E.	Reg. No. 40,594	Leffert, Thomas W.	Reg. No. 40,697	Viksnins, Ann S.	Reg. No. 37,748
Dryja, Michael A.	Reg. No. 39,662	Lemaire, Charles A.	Reg. No. 36,198	Woessner, Warren D.	Reg. No. 30,440
Embretson, Janet E.	Reg. No. 39,665	Litman, Mark A.	Reg. No. 26,390		

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Minneapolis, MN 55402

Telephone: (612) 371-2112
Facsimile: (612) 339-3061

Dated: Jan 4, 1999

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel